Analytical Probabilistic Model of Manufacturing Process Induced Variation in Weak Inversion MOSFET

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***Abstract*— In this research, the analytical probabilistic model of the drain current of the weak inversion MOSFET affected by the variation in manufacturing process has been derived. The proposed model is highly generic as it is applicable not only to the leakage current but to with arbitrary gate to source voltage. Moreover, it has been verified at nanometer level i.e. 65 nm level by using the BSIM4 based reference obtained from Monte-Carlo simulations along with the Kolmogorov-Smirnoff test and has been found to be very accurate. Hence, this research gives a knowledge extension to the semiconductor based integrated/microelectronic circuit technology area which is necessary for the analysis and design of analog/mixed signal circuits and system for signal processing.**

Keywords*— *circuit; MOSFET; process variation; signal processing; system; weak inversion

I. INTRODUCTION

Weak inversion MOSFET which is an often cited integrated/microelectronic circuit technology, has been adopted in various ultralow voltage/low power analog/mixed signal circuits and system for signal processing with inferior robustness to strong inversion device [1]. So, it is more susceptible to the process variation e.g. variation inthreshold voltage,V_{th}, channel width, W andchannel length, L etc., denoted by ΔV_{th}, ΔW and ΔL and so on. These variations become critical as technology is deeply scaled [2]. For estimating the effects of manufacturing process variation during the design phase, it is convenience to perform the analysis and modelling of process variation affected performances of MOSFET in the analytical manner. So, various previous studies on this issue have been proposed e.g. [3] which modelled ΔL induced variation in the leakage current, I_{leak} which is the drain current at zero gate to source voltage. Obviously, the drain current, I_d with arbitrary gate to source voltage, V_{gs} is not focused in this previous work. Furthermore, it has been found later that the dominant process variation of MOSFET in weak inversion is ΔV_{th} [4]. On the other hand, many analyses of variation in I_d with focusing to such dominant ΔV_{th} have been proposed e.g. [5, 6, 7] etc., under the assumption that variation in I_d is normally distributed due to the assumed linear relationship between such variation and ΔV_{th}. However, this is not the case in practice since I_d of weak inversion MOSFET and its variation are nonlinear functions of ΔV_{th} with strong nonlinearities.

Hence, the analytical probabilistic model of I_d of weak inversion MOSFET under the effect of variation in the manufacturing process has been proposed in this research. Unlike [3], the proposed model is not applicable only to I_{leak} but to I_d with arbitrary V_{gs}. Unlike [5, 6, 7], it has been found that I_d is not normally distributed. The proposed model has been verified at nanometer level i.e. 65 nm level by using the reference based on an often cited MOSFET model for computer simulation namely Berkley Short-Channel Insulated Gate Field Effect Transistor Model Version 4 i.e. BSIM4 obtained from Monte-Carlo simulations along with a powerful goodness of fit test namely the Kolmogorov-Smirnof test (KS-test) and has been found to be very accurate. So, it can be seen that this research provides a knowledge extension to the semiconductor based integrated/microelectronic circuit technology area which is a crucial foundation of the analysis and design of analog/mixed signal circuits and system for signal processing.

II. THE PROPOSED MODEL

In this section, the proposed model will be presented by starting from its derivation. For the weak inversion MOSFET, I_d which is ideally deterministic can be given by [8]

$$I_d = I_0 \frac{W}{L}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\right\} \tag{1}$$

where I_0, n and V_T stand for the pre-exponential scaling current, weak inversion slope factor and thermal voltage respectively.

By the effect of process variation which ΔV_{th} is dominant [4], I_d must be regarded as a random variable and can be redefined as in (2).

$$I_d = I_0 \frac{W}{L}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\left\{\exp\left[\frac{V_{gs}-V_{th}+\Delta V_{th}}{nV_T}\right]\right\} \quad (2)$$

Unlike [3], ΔV_{th} has been focused instead of ΔL and the probability density function of the I_d, $f_{Id}(i_d)$ where i_d denotes any sample value of I_d, can be analytically given in term of the probability density function of ΔV_{th}, $f_{\Delta Vth}(\delta V_{th})$ where δV_{th} stands for any sample value of ΔV_{th} by

$$\int_{-\infty}^{I_d} f_{I_d}(i_d)d|i_d| = \int_{-\infty}^{\Delta V_{th}} f_{\Delta V_{th}}(\delta V_{th})d|\delta V_{th}| \quad (3)$$

By using (2) and the fact that ΔV_{th} is normally distributed with zero mean and the standard deviation of $\sigma_{\Delta Vth}$ which means that

$$f_{\Delta V_{th}}(\delta V_{th}) = \frac{1}{\sqrt{2\pi}\sigma_{\Delta V_{th}}}\exp\left[-\frac{\delta V_{th}^2}{2\sigma_{\Delta V_{th}}^2}\right] \quad (4)$$

, $f_{Id}(i_d)$ can be found as

$$f_{I_d}(i_d) = \frac{nI_0W}{\sqrt{2\pi}V_T|V_{gs}-V_{th}|\sigma_{\Delta V_{th}}Li_d} \times\left[\left\{\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\right\}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\right\}^{-1} i_d\right]^{\left[-\frac{nV_T}{2\sigma_{\Delta V_{th}}}\right]} \quad (5)$$

where i_d must be greater than zero otherwise $f_{Id}(i_d) = 0$.

Since it can be seen from the proposed model that

$$\left[\left\{\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\right\}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\right\}^{-1} i_d\right]^{\left[-\frac{nV_T}{2\sigma_{\Delta V_{th}}}\right]} = \exp\left[-\frac{nV_T}{2\sigma_{\Delta V_{th}}}\ln\left[\left\{\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\right\}\left\{1-\exp\left[\frac{V_{ds}}{V_T}\right]\right\}\right\}^{-1} i_d\right]\right] \quad (6)$$

, $f_{Id}(i_d)$ is not a normal distribution function. Instead, $f_{Id}(i_d)$ states that I_d has a lognormal distribution with distribution parameters i.e. α_{Id} and β_{Id}, as given in (7) and (8). By using $f_{Id}(i_d)$, statistical parameters of I_d such as its mean, μ_{I_d} ,mode, $M(I_d)$, median, $\tilde{I}_d$ and variance, σ_{Id}^2 etc., can be analytically determined as given in (9)-(12). It can be seen from (9)-(11) that $M(I_d) < \tilde{I}_d < \mu_{Id}$. This is reasonable since I_d is a lognormal random variable.

$$\alpha_{I_d} = \frac{V_{gs}-V_{th}}{nV_T} + \ln\left[I_0\frac{W}{L}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\right] \quad (7)$$

$$\beta_{I_d} = \frac{\sigma_{\Delta V_{th}}}{nV_T} \quad (8)$$

$$\mu_{I_d} = I_0\frac{W}{L}\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}+\frac{1}{2}\left(\frac{\sigma_{\Delta V_{th}}}{nV_T}\right)^2\right]\right\}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\} \quad (9)$$

$$M(I_d) = I_0\frac{W}{L}\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\} \quad (10)$$

$$\tilde{I}_d = I_0\frac{W}{L}\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}-\frac{1}{2}\left(\frac{\sigma_{\Delta V_{th}}}{nV_T}\right)^2\right]\right\}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\} \quad (11)$$

$$\sigma_{Id}^2 = \left\{\exp\left[\left(\frac{\sigma_{\Delta V_{th}}}{nV_T}\right)^2\right]-1\right\} \left\{\left[I_0\frac{W}{L}\left\{\exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\right\}\left\{1-\exp\left[-\frac{V_{ds}}{V_T}\right]\right\}\right]^2+\exp\left[\left(\frac{\sigma_{\Delta V_{th}}}{nV_T}\right)^2\right]\right\} \quad (12)$$

Unlike [3], the proposed model is applicable not only to I_{leak} but to I_d with any V_{gs}. By letting V_{gs} be 0, the corresponding model for I_{leak} can be obtained. On the other hand, the similar model for the on current, I_{on} can be obtained by letting V_{gs} be the voltage supplied to the drain terminal of the MOSFET, V_{dd}. This is because I_{on} is I_d with $V_{gs} = V_{dd}$. In the subsequent section, the proposed model will be verified.

III. Model Verification

Verification of the proposed model has been performed at the nanometer level i.e. 65nm level by using the BSIM4 based probability density function of I_d, $f_{Id,\text{BSIM4}}(i_d)$ as the reference. Such reference can be obtained from the Monte-Carlo SPICE simulations with 2000 runs for each simulation, of the diode connected transistor circuit. For N-type MOSFET based verification, the weak inversion N-type device based diode connected transistor depicted in Fig.1 which $+V_{DD}$ and $-V_{SS}$ are the supply voltages at drain and source terminals respectively, has been used. Here, we let W = 120 nm and L = 80 nm. Moreover, $\sigma_{\Delta Vth}$ = 19.73 mV since 65nm level technology has been adopted. As a result, the comparative plot of $f_{Id}(i_d)$ (line) and $f_{Id,\text{BSIM4}}(i_d)$ (histogram) is as shown in Fig. 2 where a strong agreement between $f_{Id}(i_d)$ and $f_{Id,\text{BSIM4}}(i_d)$ can be observed. For P-type MOSFET based verification, the P-type MOSFET based diode connected transistor which can

be obtained by replacing the N-type device of the circuit in Fig. 1 by a P-type MOSFET, must be used. In this case, we also let W = 120 nm and L = 80 nm where $\sigma_{\Delta Vth}$ = 17.55 mV according to the adopted 65 nm level technology. As a result, the comparative plot of $f_{Id}(i_d)$ (line) and $f_{Id,\mathrm{BSIM4}}(i_d)$ (histogram) can be depicted as shown in Fig. 3 where a similar strong agreement between $f_{Id}(i_d)$ and $f_{Id,\mathrm{BSIM4}}(i_d)$ can also be seen.

Obviously, these agreements qualitatively verify the accuracy of the proposed model. In both figures where the lognormal distributions of I_d can be clearly observed, i_d has been normalized with respected to I_0 which is given by 66.5 μA and 59.5 μA for N-type and P-type MOSFET respectively.

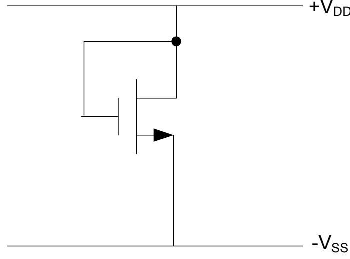

Fig.1. Weak inversion N-type MOSFET based diode connected transistor

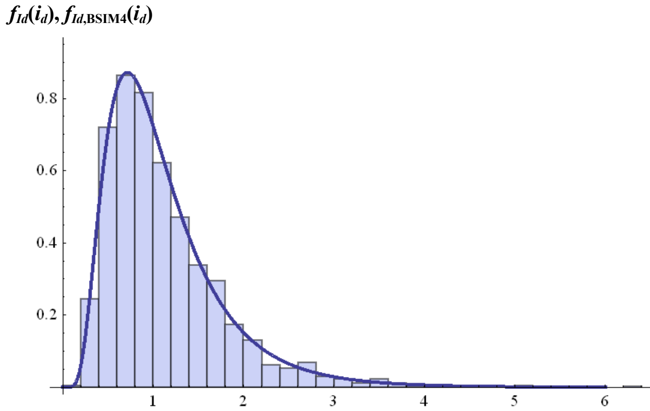

Fig.2. $f_{Id}(i_d)$ (line) and $f_{Id,\mathrm{BSIM4}}(i_d)$ (histogram): N-type MOSFET.

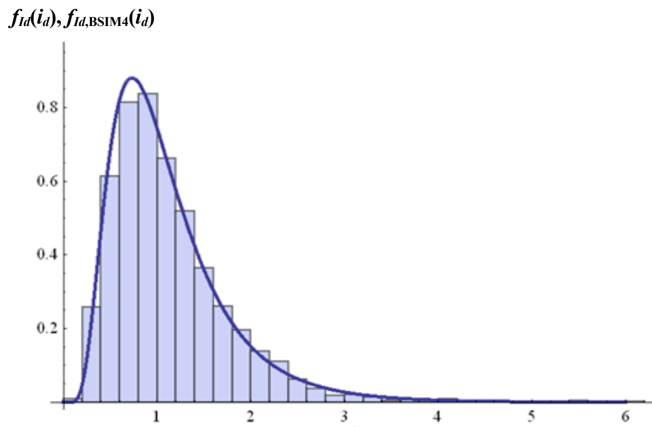

Fig.3. $f_{Id}(i_d)$ (line) and $f_{Id,\mathrm{BSIM4}}(i_d)$ (histogram): P-type MOSFET.

Since the proposed model states that I_d has a lognormal distribution, $\ln(I_d)$ is normally distributed. As a result, the KS-test which is a powerful normality test, can be applied for quantitatively verifying the proposed model via the verification of the model based distribution of $\ln(I_d)$. Since the confidence level is chosen to be 99%, the critical value, c is given by 0.0133089. For N-type MOSFET, the resulting test statistic can be found by using the data obtained from the Fig.2 as 0.0116365. Moreover, the resulting test statistic for P-type MOSFET can be obtained by using the data from the Fig.3 as 0.0116211. Since these statistics are both lower than c, it can be stated that this model can fit the simulated data with 99% confidence for both types of MOSFET. This means that the proposed model has been found to be very accurate.

IV. Discussion

In this section, some worthy of mentioned issues will be discussed. Firstly, similar models for other parameters of weak inversion MOSFET such as transconductance, g_m and drain to source conductance, g_{ds} etc., can be found by using the proposed model and principle of transformation of random variable because these parameters are functions of I_d e.g. $g_m = \partial I_d/\partial V_{gs}$ and $g_{ds} = \partial I_d/\partial V_{ds}$ *etc.*

Furthermore, this model can be used as the modelling basis of mismatch in$^{d}I_d$ of two or more MOSFETs, DI_d which can be modelled in term of its variance given by

$$Var[DI_d] = 2\sigma_{Id}^2(1-\rho_{Id}) \tag{13}$$

where ρ_{Id} denotes the correlation coefficient of I_d's of the transistors of interested. Such ρ_{Id} can be given in term of covariance of ΔV_{th} denoted by $Cov(\Delta V_{th})$ as follows

$$\rho_{Id} = \exp\left[\frac{V_{gs}-V_{th}}{nV_T}\right]\left\{\frac{\mathbf{d}\,1}{\sigma_{Idr}^2}\left\{\exp\left[\left[\frac{\sigma_{\Delta V_{th}}}{nV_T}\right]^2\left[1+\frac{Cov(\Delta V_{th})}{\sigma_{\Delta V_{th}}^2}\right]\right]\right\}\right. \\ \left. -\left\{\left\{\exp\left[\frac{1}{2}\left[\frac{\sigma_{\Delta V_{th}}}{nV_T}\right]^2\right]\right\}\right\}\left\{1-\exp\left[\frac{V_{ds}}{V_T}\right]\right\}\right\} \tag{14}$$

For closely spaced devices which are highly correlated, ρ_{Id} is maximized and $Var[DI_d]$ is minimized since $Cov(\Delta V_{th}) > 0$ [9]. For the widely spaced devices which are lowly correlated, $Cov(\Delta V_{th}) = 0$ [9], so, opposite results in ρ_{Id} and $Var[DI_d]$ are obtained. This means that best matching can be achieved for closed devices and getting worse as the distance increased.

Finally, it can be observed from the proposed model and the statistical parameters of I_d obtained by using this model such as μ_{I_d} and σ_{Id}^2 etc., that the temperature, T influences the statistical properties of I_d. For clarifying this point, μ_{Id} and σ_{Id} expressed in % of the ideal I_d which is not fluctuated, of 65nm

level devices under different T have been tabulated in Table 1 and Table 2 for N-type and P-type MOSFETs respectively. Obviously, the influence of T on both μ_{Id} and σ_{Id} can be observed where μ_{Id} is dramatically increased with increasing T. On the other hand, σ_{Id} has been found to be a decreasing function of T. It can also be seen that PMOS transistor is more robust to process variation than NMOS device according to its lower σ_{Id}.

TABLE I. STATISTICAL PARAMETERS OF DRAIN CURRENT OF 65 NANOMETER LEVEL N-TYPE MOSFETS UNDER DIFFERENT TEMPERATURES

Temperature (°C)	Statistical Parameters	
	μ_{Id} (pA)	σ_{Id} (% of I_{di})
0	1.9	54.5
30	11.8	49.1
60	52.4	44.7
90	182.4	41
120	524.8	37.9
150	1299.6	35.2
180	2854.3	32.9

TABLE II. STATISTICAL PARAMETERS OF DRAIN CURRENT OF 65 NANOMETER LEVEL P-TYPE MOSFETS UNDER DIFFERENT TEMPERATURES

Temperature (°C)	Statistical Parameters	
	μ_{Id} (pA)	σ_{Id} (% of I_{di})
0	4.9	38.1
30	27.6	34.3
60	113.5	31.2
90	369.4	28.6
120	1004.1	26.5
150	2368.5	24.6
180	4998.7	22.9

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