

Alpha Power Law Based Model of Random Variation in Nanometer FGMOSFET

Rawid Banchuin
Department of Computer Engineering
Siam University
Bangkok, Thailand

Rounsai Chaisricharoen
School of Information Technology
Mea Fah Luang University
Chaingrai, Thailand

Abstract—The alpha power law based model of random variation in drain current of an unconventional MOSFET namely Floating-Gate MOSFET (FGMOSFET) has been proposed where the nanometer level technology has been focused. The process induced device level random variations and their statistical correlations have been taken into account. The model has been found to be very accurate since it can accurately fit the 65 nm SPICE BSIM4 based reference obtained by using Monte-Carlo SPICE. So, it has been found to be efficient for the variability aware analysis and design of FGMOSFET based circuit at nanometer regime.

Keywords—alpha power law; CMOS; circuit; FGMOSFET; nanometer

I. INTRODUCTION

A special MOSFET entitled FGMOSFET has been extensively utilized in various analog/digital circuits e.g. [1]-[8] etc., which are applicable to various applications including signal processing and the nanometer CMOS technology has also been adopted. Similarly to the MOSFET based circuits, the performances of these FGMOSFET based circuits have been deteriorated by process induced device level random variations e.g. variations in threshold voltage and current factor etc., [9]-[11]. This is because these device level variations yield random variations in circuit level parameters for example, drain current (I_D) and transconductance etc., which in turn yield variations in parameters of FGMOSFET based circuit.

Similarly to MOSFET, I_D has also been found to be the key circuit level parameter of FGMOSFET as it is directly measurable and can serve as the basis for determining other circuit level parameters. According to the importance of I_D , the analytical models of process induced random variation and mismatch in I_D of MOSFET have been proposed in many previous researches for example, [12]-[14] etc., which the deeply scaled CMOS technology has also been focused. Since these works have been done without regarding to certain circuit, their results are applicable to any MOSFET based circuit including that at nanometer level. For the FGMOSFET on the other hand, it can be seen from the previous researches that most of the variability analyses have been performed in the case by case manner based on certain circuit level

parameters of certain circuits only where the micrometer CMOS technology has been focused. So, the obtain results are not generic as they are applicable only to their dedicated circuits. Moreover, the validities of these results also become suspicious if they must be applied the FGMOSFET based circuit at nanometer level. Even though a single FGMOSFET oriented variability modeling has been previously proposed in [15], this work is based on the traditional Shockley's model which is oriented to the the micrometer CMOS technology. Thus it has been found to be unfortunately inapplicable to the FGMOSFET at nanometer regime.

Motivated by these problems and the reign of the nanometer CMOS technology, the analytical model of process induced random variation in I_D (ΔI_D) of the FGMOSFET in nanometer regime has been proposed in this research by using the alpha power law [16] which has been successfully applied to the variability analysis of deeply scaled MOSFET [13], [14] as the basis. The process induced device level random variations of each region and their statistical correlations have been taken into account. This model has been formulated without regarding to any circuit. So, it is applicable to all FGMOSFET based circuits in the nanometer regime. It has been found to be very accurate since it can fit the 65 nm SPICE BSIM4 based reference obtained by using the Monte-Carlo SPICE simulation with very high accuracy. Hence, this model has been found to be an efficient tool for the variability aware analysis/design of any circuit involving FGMOSFET in the nanometer regime.

II. THE FGMOSFET

In this section, some foundations on the FGMOSFET will be summarized. According to [15], FGMOSFET is a unique variant of MOSFET with an additional gate isolated within the oxide, namely the floating gate. A cross sectional view of an N-type FGMOSFET with N inputs where $N > 1$ implemented as N discrete input gates can be shown in Fig. 1. Moreover, the symbol and equivalent circuit of an N-type N input FGMOSFET can be depicted as in Fig. 2 where $C_1, C_2, C_3, \dots, C_N, C_{fd}, C_{fs}$ and C_{fb} are respectively N input capacitances, overlap capacitance between floating-gate and drain, overlap capacitance between floating-gate and source and parasitic capacitance between floating gate and substrate.

Let $\{i\} = \{1, 2, 3, \dots, N\}$ and any i^{th} input capacitance be denoted by C_i , the floating gate voltage, V_{FG} can be given by [8], [15]

$$V_{FG} = \frac{\sum_{i=1}^N [C_i V_i] + C_{fd} V_D + C_{fs} V_S + C_{fb} V_B}{C_T} \quad (1)$$

where V_i is the input voltage at any i^{th} input gate, V_D is the drain voltage, V_S is the source voltage and V_B is the bulk voltage. Moreover, C_T denotes the total capacitance of the floating gate which can be defined as [8], [15]

$$C_T = \sum_{i=1}^N [C_i] + C_{fd} + C_{fs} + C_{fb} \quad (2)$$

Also according to [15], if we let k_i , k_{fd} , k_{fs} and k_{fb} denote the coupling factor of any i^{th} input gate, drain, source and bulk and be defined as $k_i = C_i/C_T$, $k_{fd} = C_{fd}/C_T$, $k_{fs} = C_{fs}/C_T$ and $k_{fb} = C_{fb}/C_T$ respectively, V_{FG} can be alternatively given as follows

$$V_{FG} = \sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fs} V_S + k_{fb} V_B \quad (3)$$

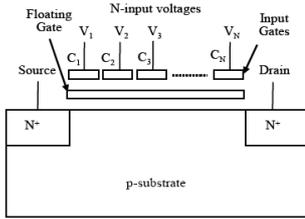


Fig. 1. A cross sectional view of N-type N input FG MOSFET [8], [15]

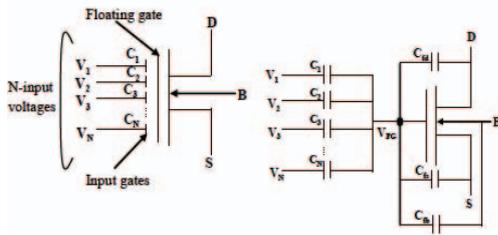


Fig. 2. The symbol (left) and equivalent circuit model (right) of an N-type N input FG MOSFET [8], [15]

In the subsequent section, the proposed model will be derived.

III. THE PROPOSED MODEL

Before proceed further, I_D of the nanometer FG MOSFET must be firstly formulated. With the alpha power law, I_D of the ordinary nanometer MOSFET can be given by

$$I_D = \frac{\beta}{2} (V_{GS} - V_{TH})^\alpha \quad (4)$$

where V_{GS} , V_{TH} , α and β denote the gate to source voltage, threshold voltage, velocity saturation index and current factor respectively.

For the obtaining the I_D of FG MOSFET, V_{GS} in (4) must be replaced by $V_{FG} - V_S$. By combing (3) and (4) and keeping in mind that $k_{fs} \ll 1$, I_D of nanometer FG MOSFET is

$$I_D = \frac{\beta}{2} \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^\alpha \quad (5)$$

From (5), it can be seen that the effect of the source coupling factor is insignificant compared to the others and the process induced device level random variations i.e. the random variations in V_{TH} , α , β , k_i , k_{fd} and k_{fb} denoted by ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} respectively. So, ΔI_D of the nanometer multiple input FG MOSFET in triode region can be given by (6) where all derivatives can be determined by using (5) as given by (7)-(12).

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{TH}} \right) \Delta V_{TH} + \left(\frac{\partial I_D}{\partial \alpha} \right) \Delta \alpha + \left(\frac{\partial I_D}{\partial \beta} \right) \Delta \beta + \left(\frac{\partial I_D}{\partial k_{fd}} \right) \Delta k_{fd} + \left(\frac{\partial I_D}{\partial k_{fb}} \right) \Delta k_{fb} + \sum_{i=1}^N \left[\left(\frac{\partial I_D}{\partial k_i} \right) \Delta k_i \right] \quad (6)$$

$$\frac{\partial I_D}{\partial V_{TH}} = -\frac{\alpha \beta}{2} \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^{\alpha-1} \quad (7)$$

$$\frac{\partial I_D}{\partial \alpha} = \frac{\beta}{2} \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^\alpha \times \ln \left[\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right] \quad (8)$$

$$\frac{\partial I_D}{\partial \beta} = \frac{1}{2} \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^\alpha \quad (9)$$

$$\frac{\partial I_D}{\partial k_{fd}} = \frac{\alpha \beta}{2} V_D \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^{\alpha-1} \quad (10)$$

$$\frac{\partial I_D}{\partial k_{fb}} = \frac{\alpha\beta}{2} V_B \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^{\alpha-1} \quad (11)$$

$$\rho_{\Delta x, \Delta y} = \frac{E[\Delta x \Delta y]}{\sqrt{\sigma_{\Delta x}^2} \sqrt{\sigma_{\Delta y}^2}} \quad (14)$$

$$\frac{\partial I_D}{\partial k_i} = \frac{\alpha\beta}{2} V_i \left(\sum_{i=1}^N [k_i V_i] + k_{fd} V_D + k_{fb} V_B - V_S - V_{TH} \right)^{\alpha-1} \quad (12)$$

Since ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} are random variables, so does ΔI_D and the statistical parameters of ΔI_D must be derived for the complete modeling. In order to do so, the average and variance of ΔI_D i.e. $\Delta I_{D,avr}$ and $\sigma_{\Delta I_D}^2$, must be formulated. As a result, $\Delta I_{D,avr} = 0$ similar to those of ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} . However, $\sigma_{\Delta I_D}^2$ is nonzero because the variances of ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} are not. By also taking the statistical correlations of ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} into account, $\sigma_{\Delta I_D}^2$ can be analytically given by (13) where $\rho_{\Delta x, \Delta y}$ for example, $\rho_{\Delta V_{TH}, \Delta\beta}$, $\rho_{\Delta\alpha, \Delta\beta}$ and $\rho_{\Delta V_{TH}, \Delta\alpha}$ etc., denotes the correlation coefficient of Δx and Δy and displays their degree of statistical correlation. Moreover, $\sigma_{\Delta V_{TH}}^2$, $\sigma_{\Delta\alpha}^2$, $\sigma_{\Delta\beta}^2$, $\sigma_{\Delta k_i}^2$, $\sigma_{\Delta k_{fd}}^2$ and $\sigma_{\Delta k_{fb}}^2$ respectively denote the variances of ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_i , Δk_{fd} and Δk_{fb} . Finally, it can be seen that the 1st up to 6th term of (13) are induced by $\sigma_{\Delta V_{TH}}^2$, $\sigma_{\Delta\alpha}^2$, $\sigma_{\Delta\beta}^2$, $\sigma_{\Delta k_i}^2$, $\sigma_{\Delta k_{fd}}^2$ and $\sigma_{\Delta k_{fb}}^2$ respectively where the others have been caused by the statistical correlations. Before proceed further, it should be mentioned here that $\rho_{\Delta x, \Delta y}$ can be obtained by using (14) where $E[\]$ stands for the expectation operator. In the subsequent section, the accuracy of the proposed model will be verified.

$$\begin{aligned} \sigma_{\Delta I_D}^2 = & \left(\frac{\partial I_D}{\partial V_{TH}} \right)^2 \sigma_{\Delta V_{TH}}^2 + \left(\frac{\partial I_D}{\partial \alpha} \right)^2 \sigma_{\Delta \alpha}^2 + \left(\frac{\partial I_D}{\partial \beta} \right)^2 \sigma_{\Delta \beta}^2 + \left(\frac{\partial I_D}{\partial k_{fd}} \right)^2 \sigma_{\Delta k_{fd}}^2 \\ & + \left(\frac{\partial I_D}{\partial k_{fb}} \right)^2 \sigma_{\Delta k_{fb}}^2 + \sum_{i=1}^N \left(\frac{\partial I_D}{\partial k_i} \right)^2 \sigma_{\Delta k_i}^2 + 2 \left(\frac{\partial I_D}{\partial \alpha} \right) \left(\frac{\partial I_D}{\partial V_{TH}} \right) \rho_{\Delta \alpha, \Delta V_{TH}} \sqrt{\sigma_{\Delta \alpha}^2} \sqrt{\sigma_{\Delta V_{TH}}^2} \\ & + 2 \left(\frac{\partial I_D}{\partial \beta} \right) \left(\frac{\partial I_D}{\partial V_{TH}} \right) \rho_{\Delta \beta, \Delta V_{TH}} \sqrt{\sigma_{\Delta \beta}^2} \sqrt{\sigma_{\Delta V_{TH}}^2} + 2 \left(\frac{\partial I_D}{\partial V_{TH}} \right) \left(\frac{\partial I_D}{\partial k_{fd}} \right) \rho_{\Delta V_{TH}, \Delta k_{fd}} \sqrt{\sigma_{\Delta V_{TH}}^2} \sqrt{\sigma_{\Delta k_{fd}}^2} \\ & + 2 \left(\frac{\partial I_D}{\partial V_{TH}} \right) \left(\frac{\partial I_D}{\partial k_{fb}} \right) \rho_{\Delta V_{TH}, \Delta k_{fb}} \sqrt{\sigma_{\Delta V_{TH}}^2} \sqrt{\sigma_{\Delta k_{fb}}^2} + 2 \sum_{i=1}^N \left(\frac{\partial I_D}{\partial V_{TH}} \right) \left(\frac{\partial I_D}{\partial k_i} \right) \rho_{\Delta V_{TH}, \Delta k_i} \sqrt{\sigma_{\Delta V_{TH}}^2} \sqrt{\sigma_{\Delta k_i}^2} \\ & + 2 \left(\frac{\partial I_D}{\partial \alpha} \right) \left(\frac{\partial I_D}{\partial \beta} \right) \rho_{\Delta \alpha, \Delta \beta} \sqrt{\sigma_{\Delta \alpha}^2} \sqrt{\sigma_{\Delta \beta}^2} + 2 \left(\frac{\partial I_D}{\partial \alpha} \right) \left(\frac{\partial I_D}{\partial k_{fd}} \right) \rho_{\Delta \alpha, \Delta k_{fd}} \sqrt{\sigma_{\Delta \alpha}^2} \sqrt{\sigma_{\Delta k_{fd}}^2} \\ & + 2 \left(\frac{\partial I_D}{\partial \alpha} \right) \left(\frac{\partial I_D}{\partial k_{fb}} \right) \rho_{\Delta \alpha, \Delta k_{fb}} \sqrt{\sigma_{\Delta \alpha}^2} \sqrt{\sigma_{\Delta k_{fb}}^2} + 2 \sum_{i=1}^N \left(\frac{\partial I_D}{\partial \alpha} \right) \left(\frac{\partial I_D}{\partial k_i} \right) \rho_{\Delta \alpha, \Delta k_i} \sqrt{\sigma_{\Delta \alpha}^2} \sqrt{\sigma_{\Delta k_i}^2} \\ & + 2 \left(\frac{\partial I_D}{\partial \beta} \right) \left(\frac{\partial I_D}{\partial k_{fd}} \right) \rho_{\Delta \beta, \Delta k_{fd}} \sqrt{\sigma_{\Delta \beta}^2} \sqrt{\sigma_{\Delta k_{fd}}^2} + 2 \left(\frac{\partial I_D}{\partial \beta} \right) \left(\frac{\partial I_D}{\partial k_{fb}} \right) \rho_{\Delta \beta, \Delta k_{fb}} \sqrt{\sigma_{\Delta \beta}^2} \sqrt{\sigma_{\Delta k_{fb}}^2} \\ & + 2 \sum_{i=1}^N \left(\frac{\partial I_D}{\partial \beta} \right) \left(\frac{\partial I_D}{\partial k_i} \right) \rho_{\Delta \beta, \Delta k_i} \sqrt{\sigma_{\Delta \beta}^2} \sqrt{\sigma_{\Delta k_i}^2} + 2 \left(\frac{\partial I_D}{\partial k_{fd}} \right) \left(\frac{\partial I_D}{\partial k_{fb}} \right) \rho_{\Delta k_{fd}, \Delta k_{fb}} \sqrt{\sigma_{\Delta k_{fd}}^2} \sqrt{\sigma_{\Delta k_{fb}}^2} \\ & + 2 \sum_{i=1}^N \left(\frac{\partial I_D}{\partial k_{fb}} \right) \left(\frac{\partial I_D}{\partial k_i} \right) \rho_{\Delta k_{fb}, \Delta k_i} \sqrt{\sigma_{\Delta k_{fb}}^2} \sqrt{\sigma_{\Delta k_i}^2} + 2 \sum_{i=1}^N \left(\frac{\partial I_D}{\partial k_{fd}} \right) \left(\frac{\partial I_D}{\partial k_i} \right) \rho_{\Delta k_{fd}, \Delta k_i} \sqrt{\sigma_{\Delta k_{fd}}^2} \sqrt{\sigma_{\Delta k_i}^2} \\ & + \sum_{j=1}^N \sum_{i=1}^N \left(\frac{\partial I_D}{\partial k_i} \right) \left(\frac{\partial I_D}{\partial k_j} \right) \rho_{\Delta k_i, \Delta k_j} \sqrt{\sigma_{\Delta k_i}^2} \sqrt{\sigma_{\Delta k_j}^2} \end{aligned} \quad (13)$$

IV. MODEL VERIFICATION

Verification of the proposed model will be performed based on the N-type FG MOSFET with $N = 2$, $k_1 = k_2 = 0.5$, SPICE BSIM4 and 65 nm CMOS technology. Noted also that the channel length and the aspect ratio of 65 nm and 4/3 have been used. For performing the verification, the root mean square (rms.) value of ΔI_D calculated by using the model ($\Delta I_{D,rms,M}$) has been graphically compared to its SPICE BSIM4 based reference ($\Delta I_{D,rms,SPICE}$) obtained by using the Monte-Carlo SPICE simulation with 1000 runs. For convenience, ΔV_{TH} , $\Delta\alpha$, $\Delta\beta$, Δk_1 and Δk_2 have been assumed to be normally distributed where all $\rho_{\Delta x, \Delta y}$'s have been assumed to be 0.5 as this value is a reasonable estimation [17].

Moreover, the SPICE BSIM4 based modelling of the FG MOSFET with $N = 2$ can be performed by using the two inputs version of the equivalent circuit depicted in Fig. 2 where the core MOSFET has been modelled by using the SPICE BSIM4. Both $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ have been expressed as percentage of their corresponding nominal drain currents and comparatively plotted against the magnitude of the voltage of the 1st and 2nd input denoted by $|V_1|$ and $|V_2|$ respectively. It should be mentioned here that $|V_2| = 0$ V in the comparative plots with respected to $|V_1|$ and vice versa. Here we let $\sigma_{\Delta V_{TH}} / V_{TH} = \sigma_{\Delta \alpha} / \alpha = \sigma_{\Delta \beta} / \beta = \sigma_{\Delta k_1} / k_1 = \sigma_{\Delta k_2} / k_2 = 0.01$ as we assume that V_{TH} , α , β , k_1 and k_2 have 1% variation. As results, the comparative plots of $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ against $|V_1|$ where $|V_2| = 0$ and vice versa can be respectively shown in Fig. 3 and 4 where highly strong agreements between $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ which are respectively drawn as normal curves and dotted curves, can be observed. Moreover, the average deviation between $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ determined from both figures has been found to be 5.65% which is notably very small. So, the the proposed model has been found to be very accurate.

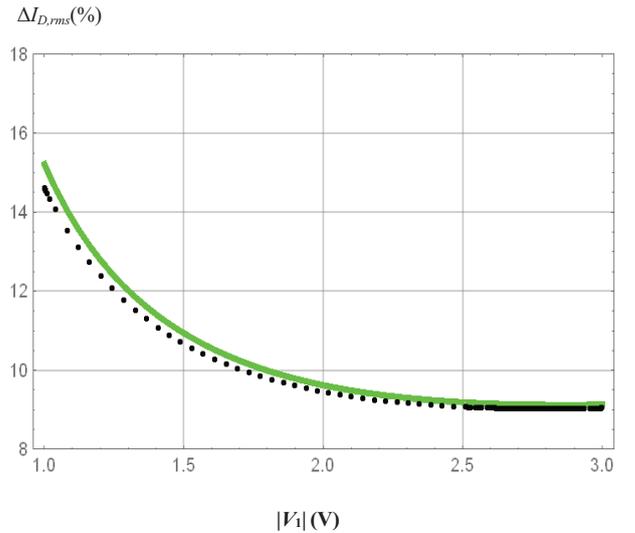


Fig. 3. The comparative plots of $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ against $|V_1|$

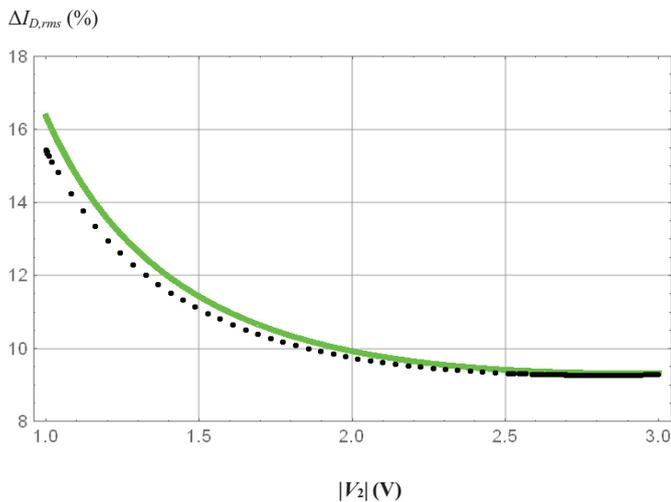


Fig. 4. The comparative plots of $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ against $|V_2|$

V. CONCLUSION

In this research, the analytical model of ΔI_D of the FGMOSFET has been proposed based on the up to dated alpha power law as the nanometer level technology has been focused. The process induced device level random variations and their statistical correlations have been taken into account. The proposed model has been found to be very accurate since it can fit the 65 nm SPICE BSIM4 based reference obtained by using Monte-Carlo simulation with considerable very small average deviations. So, this work has been found to be beneficial to the variability aware analysis/designing of any FGMOSFET circuit in the nanometer regime which employs many applications including signal processing. As a further study, the similar modeling of triode region operated nanometer FGMOSFET should be performed as this work is focused on this device in saturated region.

ACKNOWLEDGMENT

The author would like to acknowledge Mahidol University, Thailand, for the online database service.

REFERENCES

- [1] S.K. Saha, "Design considerations for sub-90 nm split-gate flash memory cells," *IEEE Trans. Electron Dev.*, vol. 54, pp. 3049-3055, November 2007.
- [2] S.K. Saha, "Scaling considerations for sub-90 nm split-gate flash memory cells," *IET Circ. Device Syst.*, vol. 2, pp. 144-150, February 2008
- [3] C-W. Cao, S-G. Zang, X. Lin, Q-Q. Sun, C. Xing, P-F. Wang, and D. W. Zhang, "A novel 1T-1D DRAM cell for embedded application," *IEEE Trans. Electron Dev.*, vol. 59, pp. 1304-1310, May 2012.
- [4] C. Y. Kwok and H. R. Merhrvarz, "Low voltage and mismatch analysis of quadruple source coupled multi-input floating-gate MOSFET multiplier with offset trimming," *Analog Integr. Circuits Signal Process.*, vol. 26, pp. 141-156, February 2001.
- [5] S. Vlassis and S. Siskos, "Design of voltage-mode and current-mode computational circuits using floating-gate MOS transistors," *IEEE Trans. Circuits Syst. I, Reg. Papers.*, vol. 51, pp. 329-341, February 2004.
- [6] S. Vlassis and S. Siskos, "Differential-voltage attenuator based on floating-gate MOS transistors and its applications," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, pp. 1372-1378, November 2001.
- [7] Y. Zhai and P. A. Abshire, "Adaptive log domain filters for system identification using floating gate transistors," *Analog Integr. Circuits Signal Process.*, vol.56, pp.23-36, August 2008.
- [8] R. Pandey and M. Gupta, "FGMOS based voltage-controlled grounded resistor," *RADIOENGINEERING*, vol. 19, pp. 455-459, September 2010.
- [9] M.J.M. Pelgrom, A.C.J. Duinmaijer and A.P.G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433-1440, October 1989.
- [10] S.K. Saha, "Modelling process variability in scaled CMOS technology," *IEEE Des. Test Comput.*, vol. 27, pp. 8-16, March-April 2010.
- [11] K. Kelin, "Variability in nanoscale CMOS technology," *SCIENCE CHINA Information Sciences*, vol. 54, pp 936-945, May 2011.
- [12] P.R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1212- 1224, June 2005.
- [13] H. Masuda, T. Kida and S. Ohkawa, "Comprehensive matching characterization of analog CMOS circuits," *IEICE Trans. Fund. Electron. Comm. Comput. Sci.*, vol. E92-A, pp. 966-975, April 2009.
- [14] K. Hasegawa, M. Aoki, T. Yamawaki, S. Tanaka, "Modeling transistor variation using α -power formula and its application to sensitivity analysis on harmonic distortion in differential amplifier," *Analog Integr. Circuits Signal Process.*, vol. 72, pp. 605-613, June 2011.
- [15] R. Banchuin, "Analytical model of random variation in drain current of FGMOSFET," *Act. passive electron. compon.*, vol. 2015, pp. 1-12, July 2015.
- [16] S. Takayasu, and A.R. Newton. "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, pp. 584-594, April 1990.
- [17] K. Khu, "Statistical modeling for Monte-Carlo simulation using HSPICE," *Proc. 2006 SNUG Conf.*, pp 1-10, 2006.